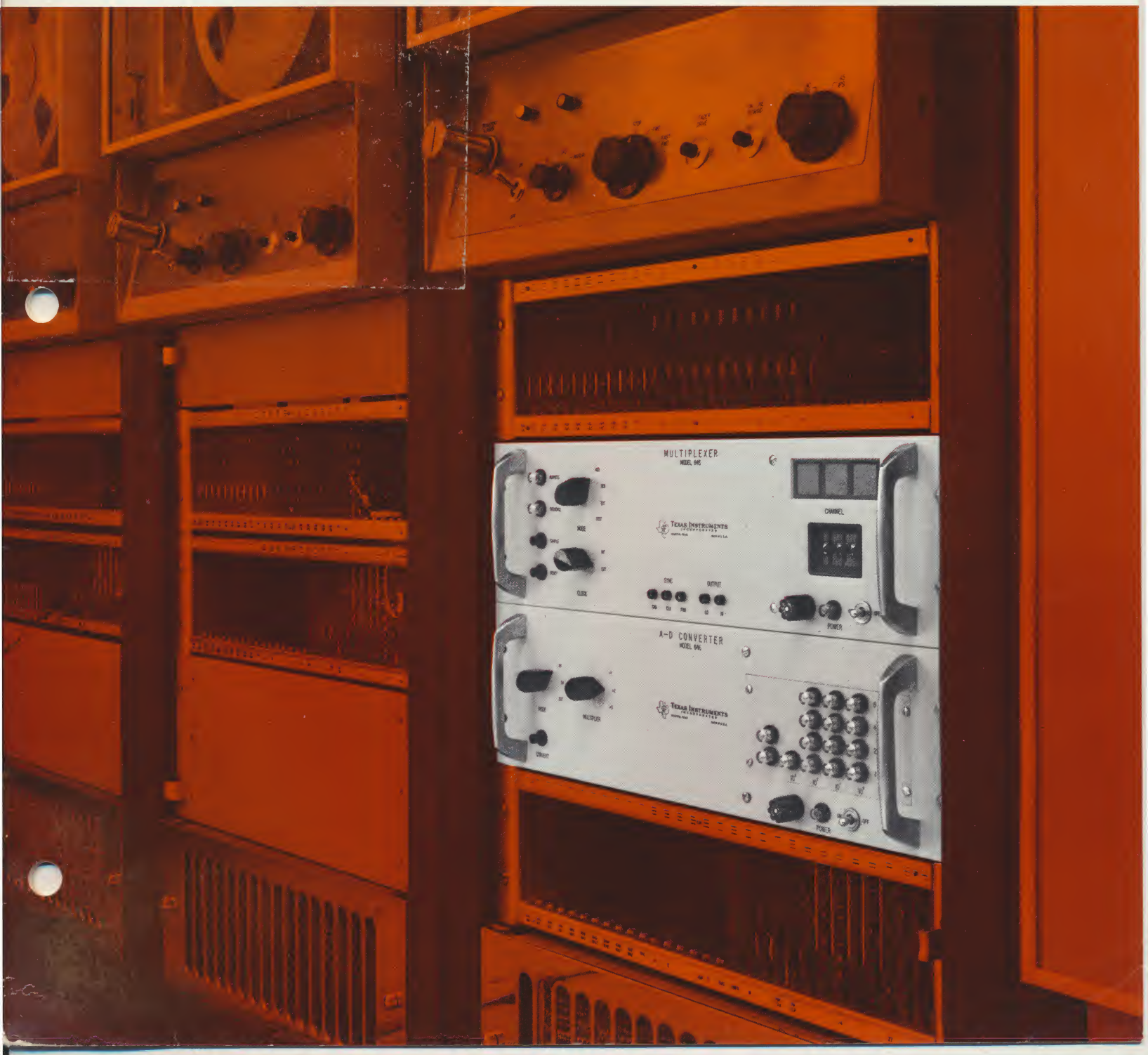
TEXAS INSTRUMENTS

SERIES 800

T1-702-2.5M.366

analog to digital converters, multiplexers and digital to analog converters



SERIES 846

analog to digital converters

- High Speed—over 50,000 conversions/sec
- Built-in Sample and Hold—100 nanosecond aperture
- High Accuracy—to ± 0.025% full scale at 57 KC with sample and hold
- Binary or BCD Output Codes
- 100 Megohm Input Impedance—single-ended or differential

Texas Instruments Analog to Digital Converters are versatile all solid-state instruments combining high speed with high accuracy. These units are successive approximation, feedback voltage encoders, utilizing a built-in precision reference. All Series 846 Converters include an integral sample and hold circuit with a 100 nanosecond aperture. The best in accurate digitization of dc, time-varying, or pulse amplitude analog inputs is the objective of TI's approach to sample and hold and the associated *automatic zero stabilization.*

Modular construction allows a wide choice of input/output specifications, as shown in the diagram below. Additional system integration flexibility is provided by transformer-coupled control signals and auxiliary outputs.

modeling code

DETAIL SPECIFICATIONS AND MODEL DESIGNATION

MODEL NUMBER 846-XXX-XXX-XX A-D CONVERTER

BASIC SERIES

BASIC SPEED AND ACCURACY INCLUDING SAMPLE AND HOLD			
OUTPUT INCLUDING SIGN	MAXIMUM CONVERSION RATE PER SECOND	ACCURACY ± ½ LSB	CODE
13 bit BCD 8421	57 KC	± 0.05% FS	A
14 bit BCD 8421	54 KC	± 0.05% FS	B
15 bit BCD 8421	51 KC	± 0.025% FS	C
13 binary bits	57 KC	± 0.025% FS	D
12 binary bits	60 KC	± 0.05% FS	E
11 binary bits	64 KC	± 0.05% FS	F
10 binary bits	69 KC	± 0.05% FS	G

INPUT TYPE	CODE
Single-ended	1
Differential	2

MODE	CODE
AD	A
ADA—High impedance output	B
ADA—Low impedance output	C

LOGIC LEVELS		CODE
"1"	"0"	
+6 v	0 v	01
0 v	+6 v	02
−6 v	0 v	03
0 v	−6 v	04
+10 v	0 v	11
0 v	+10 v	12
−10 v	0 v	13
0 v	−10 v	14

FRONT PANEL DISPLAY	CODE
1 light per bit	A
NIXIE® (BCD Models Only)	B

OUTPUT CODE	CODE
Sign and Absolute Value	A
Offset Straight Binary*	B
One's Complement*	C
Two's Complement*	D
Unipolar**	E

*Binary models only
**12 Binary bits maximum

INPUT VOLTAGE RANGE	CODE
± 10 v	1
± 8.190 v	2
± 5 v	3
± 4.095 v	4
± 2.5 v	5
± 2.0475 v	6
Multi ± 1, 3, 10 (A model only)	7
Multi ± 2, 4, 10 (B, C models only)	8
Multi ± 2.5, 5, 10 (Binary models only)	9
Multi ± 2.0475, 4.095, 8.190 (Binary models only)	0

specifications

BASIC SPEED AND ACCURACY COMBINATIONS including sample and hold:

Type	Output Code	Number of Bits Including Sign	Accuracy ± ½ lsb	Linearity	Maximum Conversion Rate
A	BCD 8421	13	± 0.05% FS	± 0.025% FS	57,000 conv/sec
B		14	± 0.05% FS	± 0.025% FS	54,000 conv/sec
C		15	± 0.025% FS	± 0.01% FS	51,000 conv/sec
D	Binary, all versions	13	± 0.025% FS	± 0.01% FS	57,000 conv/sec
E		12	± 0.05% FS	± 0.025% FS	60,000 conv/sec
F		11	± 0.05% FS	± 0.025% FS	64,000 conv/sec
G		10	± 0.05% FS	± 0.025% FS	69,000 conv/sec

STABILITY: ± ½ bit drift, 90 day period

ANALOG SIGNAL INPUT:

Input Impedance:
1. Standard, >100 megohms shunted by <25 pf, single-ended
2. Optional, >100 megohms shunted by <25 pf, differential
   Each leg to ground, >100 megohms shunted by <25 pf.

Sample and Hold: (Standard, all models)
- Sample Time: 3 microsecond
- Aperture Time: 100 nanosecond

Signal Voltage Range: See Model Designation Chart

Common Mode: (Differential inputs only)
- Rejection: ≥66 db, dc to 1000 cps, with 1000 ohms source unbalance.
- Common Mode Voltage Max: For normal operation, the algebraic sum of common mode voltage plus differential signal voltage should not exceed twice the input range or ± 12 volts, whichever is less.
- Impedance to Ground: 10,000 ohms max.

Overvoltage: Up to 100% overvoltage on any range. Signal, including common mode voltage, may not exceed on any range — ± 40 volts for 1 sec, ± 20 volts indefinitely. Note: Input impedance is 1000 ohms for inputs over ± 12 v.

DIGITAL DATA OUTPUTS:

Parallel: Logic levels and output codes as given in Model Designation Chart. All levels ± 1 v tolerance at ± 3 ma max. Output levels remain until next *Convert Command*.

Serial: Modulated pulse train produced during conversion cycle at nominal 1 mc internal clock rate, transformer-coupled, isolated from instrument ground.
1 = no pulse, 0 = pulse.
- Amplitude: 7 v ± 1 v at 5 ma for 10% droop.
- Rise Time: ≤50 nsec
- Pulse Width: 120 ± 50 nsec
- Output Impedance: ≤70 ohms, dynamic.

CONTROL SIGNAL INPUT REQUIRED (from customer):

Convert Command: Manual: Push-button, single conversion.
External: Positive or negative-going pulse or level change, transformer-coupled input, isolated from instrument ground.
- Input Impedance: 0.02 μf in series with approximately 700 ohms, dynamic
- Amplitude: 2 v min, 10 v max
- Rise Time: ≤1.0 μsec
- Pulse Width: ≥0.2 μsec

CONTROL SIGNAL OUTPUTS (to customer):

Digitization Complete: A true or "1" level occurring synchronously with establishment of least significant (last) bit.

Auxiliary Control: A 1.0 μsec true signal. Can occur at any increment of 1.0 μsec before *Digitization Complete*. Normally wired to occur 3.0 μsec prior. Same logic level as Parallel Data Output.

Internal Clock: Pulse train produced during conversion cycle at nominal 1 mc rate, transformer-coupled pulse output, isolated from instrument ground.
- Amplitude: 7 v ± 1 v @ ± 5 ma
- Rise Time: ≤50 nsec
- Pulse Width: 120 ± 50 nsec
- Fall Time: ≤50 nsec
- Output Impedance: ≤70 ohms, dynamic

FRONT PANEL DISPLAY: Standard: Neon indicators for sign and each bit.
Optional: BCD units, NIXIE® decimal indicators for sign and each digit.

OPERATING TEMPERATURE: 0 to +55°C

POWER: 105-125 vrms, 48-62 cps, single phase, 75 watts. 230 vrms available option.

DIGITAL-ANALOG OPTION:

DA Conversion Rate: >200 KC

Digital Signal Input: A true or "1" level. Parallel single rail, direct coupled. Levels must be established at least 1.0 μsec before *DA Command* and remain until completion of *DA Command*.

DA Command Input: A true or "1" pulse. Direct coupled. Minimum width 1.0 μsec.

Analog Signal Output: NRZ, all units.

High Impedance: Directly from DAC network.
- Voltage:
  - Binary models: nominally ± 4 volts
  - BCD models: nominally ± 2.5 volts
- Output Impedance: Precision resistance, nominally 1 K ohm, depending on model.

Low Impedance: Buffered through amplifier
- Voltage: Determined by AD range
- Settling Time: To ± 0.1% final value in <4 μsec
- Output Impedance: ≤1 ohm

controls and control signals

SERIES 846

MULTIPLIER (Range) Switch (Multi-Range Units Only) In AD mode, selects input voltage range of instrument. In ADA mode, with buffer amplifier only, selects output voltage range.

MODE Switch (ADA only) Selects mode of operation: AD, DA, or EXTernal (REMOTE) Control.

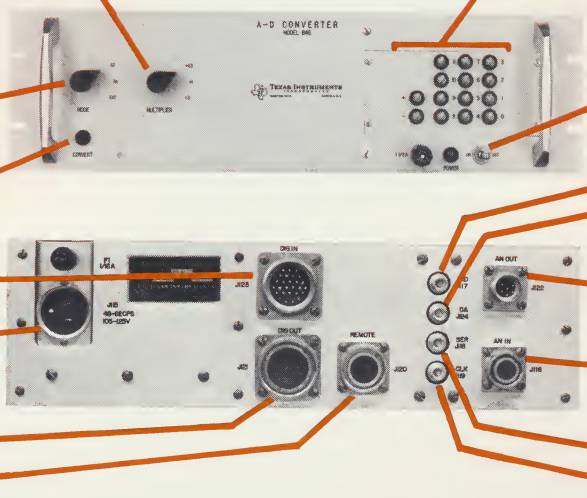
CONVERT Push-button Initiates a single conversion anytime the instrument is in the AD mode.

Parallel Digit Input (ADA units only)

A-C Line—3 prong a-c power connector

Parallel Digit Output

Remote: AD-DA and Range Select Inputs



Indicator Panel In conjunction with selected MULTIPLIER, displays result of conversion. (Binary display shown. NIXIE® display optional in BCD units).

Power—An "off-on" switch located on the front panel with power fuse and pilot lamp.

AD Command

DA Command (ADA units only)

Analog Output (ADA units only)

Analog Input

Serial Digit Output

Bit Clock Output

built-in sample and hold...

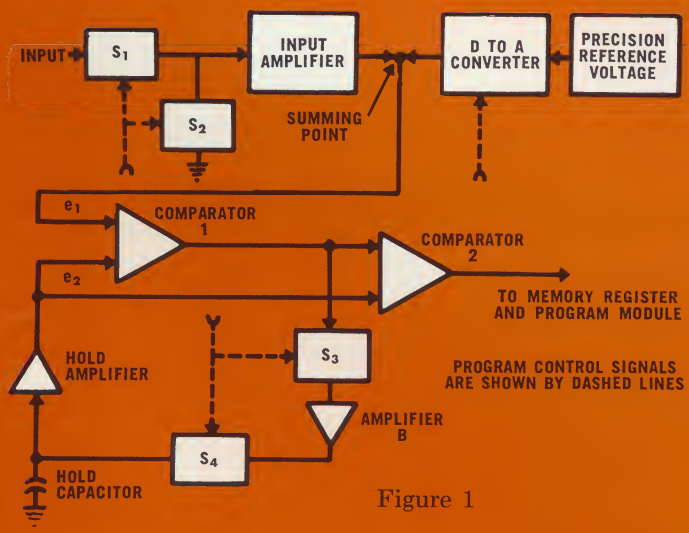


Figure 1

When the sampling process begins, upon receipt of a command signal, the d-a converter in Fig. 1 is set to zero output and switches numbered 1 through 4 are set as follows: S_1 closed, S_2 open, S_3 closed and S_4 closed. The input voltage is thus applied to the input amplifier. Output of this amplifier is summed with the d-a output (now zero) and fed to comparator 1. Also included in this comparator input voltage are any offset errors accumulated in S_1 and the input amplifier. The total signal—input voltage plus errors—drives a feedback loop through S_3, amplifier B, S_4 and the hold amplifier. By this action the hold capacitor is charged until inputs e_1 and e_2 at comparator 1 are equal. The hold-capacitor voltage is effectively equal to the input signal plus offset errors.

At this point, 3 μsec after the command signal occurs, a program command reverses switches 1 through 4 in the order S_4, S_3, S_1 and finally S_2. This switching sequence prevents transients from affecting hold-capacitor charge and represents most of the 100 nsec aperture time. The 3 μsec period is sufficient to insure proper tracking even for full-range input signal reversals.

The feedback loop that charged the hold capacitor is now open and the input signal disconnected. Switch S_2 is trimmed so its offset error matches S_1. Thus e_1 at comparator 1 input will include the same offset errors present during sampling, plus whatever output is generated by the d-a converter. Input e_2 is the sampled input voltage, now trapped, plus offset errors. Polarities are such that offset errors are opposed and eliminated during subsequent digitization. This provides *automatic zero stabilization.*

A similar cancellation scheme is used at comparator 2, but for a different reason. Inherent in the basic comparator circuit is some nonlinearity. To achieve 0.025 per cent accuracy the effect of such distortion must be removed. Differential action of comparator 2 achieves the desired results.

The only stabilizing element within the unity gain loop is the hold capacitor. There are no time delay elements elsewhere in the circuit. It is primarily for this reason that an aperture time of 100 nanoseconds is achieved.

available output codes

OFFSET BINARY

+Full Scale = 111111111111
Zero = 100000000000
−Full Scale = 000000000000

ONE'S COMPLEMENT

+Full Scale = 011111111111
Zero = 000000000000
−Full Scale = 100000000000

TWO'S COMPLEMENT

+Full Scale = 011111111111
Zero = 000000000000
−Full Scale = 100000000001

SIGN & ABSOLUTE VALUE

+Full Scale = 011111111111
Zero = 000000000000
−Full Scale = 111111111111

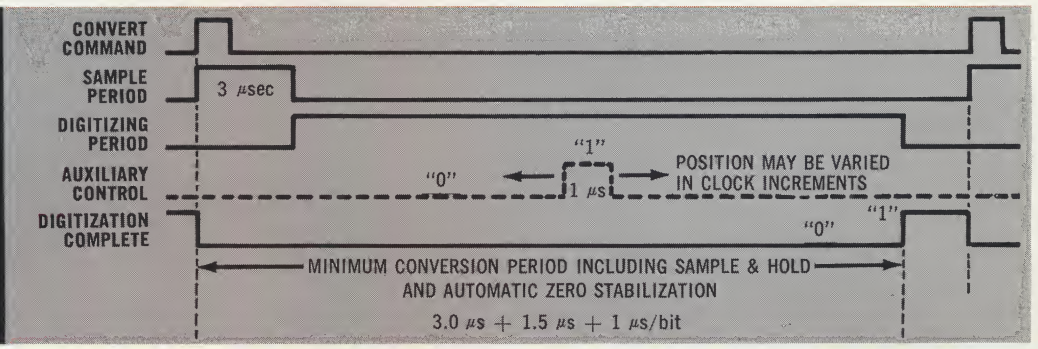
STRAIGHT BINARY (UNIPOLAR)

+Full Scale = 111111111111
Zero = 000000000000

BINARY CODED DECIMAL
8421 code: positive="0" negative="1"

	846A	846B	846C
+Full Scale	+999	+1,999	+3,999
Zero	+000	+0,000	+0,000
−Full Scale	−999	−1,999	−3,999

basic timing diagram series 846



minimum aperture time...

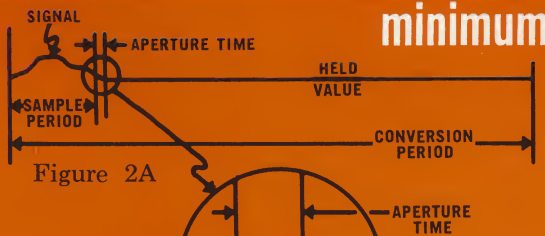


Figure 2A

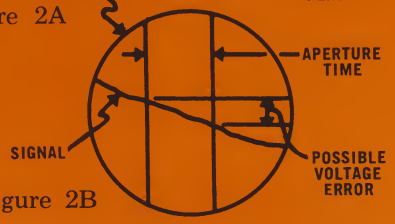
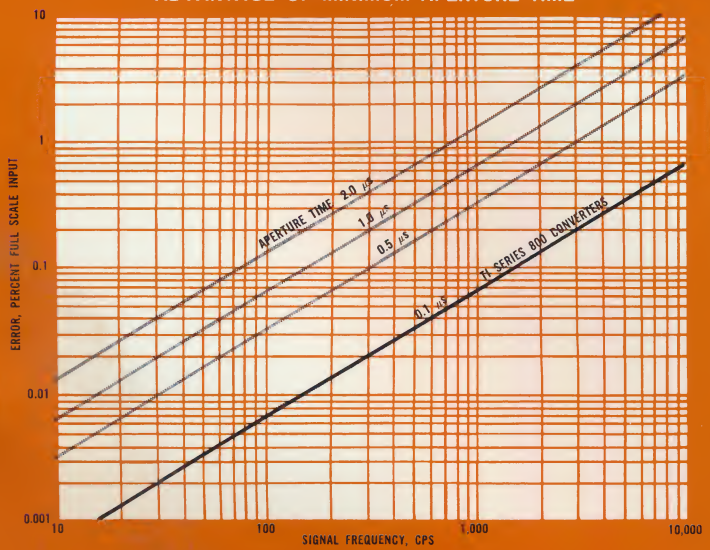


Figure 2B

ADVANTAGE OF MINIMUM APERTURE TIME



For digitization of varying or short duration (pulse) input signals, a sample-and-hold capability is a well-known requirement; for the most accurate digitization of varying inputs, a sample-and-hold with *minimum aperture time* must be employed. Figure 2A shows where sample period and aperture time normally occur in a conversion cycle. During the sample period, a sampling circuit is made to track fluctuations in the input signal; at the end of the sample period, the value in the sampling circuit is trapped and held for subsequent digitization. The signal value held for digitization may differ from the input signal within limits determined by aperture time and signal frequency (see graph).

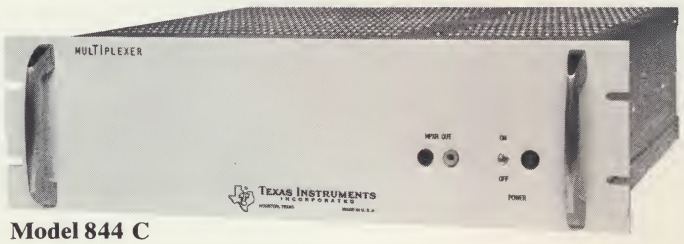
Aperture time is a two-part measure of dynamic tracking accuracy. It is comprised of phase (or time) lag inherent in finite band-width tracking circuits, and disconnect time uncertainty caused by jitter and finite switch operating time. The effect can be considered an amplitude error for a given time or a time error for a given amplitude (see Fig. 2B).

As a result of careful design of the analog sampling and comparator circuits, an extremely short aperture time (100 nanoseconds) is provided in all Series 800 AD Converters.

SERIES 844 AND 845

multiplexers

Model 845 E



Model 844 C

- Addressable, sequential, addressable/sequential combined, and direct select
- Sampling to 50,000 channels/sec
- Variable frame length
- Linearity ± 0.01% full scale

Series 844 and 845 Time Division Multiplexers are versatile all solid-state units offering accurate, high-speed, bipolar switching. Linearity is ± 0.01% of full scale—at 50,000 channels per second sampling rate. They are available in four versions: addressable, sequential, combination addressable and sequential, and direct channel select. The units offer low dynamic crossfeed, fast settling time and variable sampling duration. All models (except direct select) feature in-line display of the selected channel number, manual channel select switches for system setup and check-out, electrical channel confirmation output, and in sequential mode, front panel control of frame length. The 844 Series use binary coded decimal logic (8421 code) for addressing and are available with any increment of 10 channels up to a maximum of 100. The 845 Series accommodate up to 160 channels in any increment of 16 and are addressable in straight binary code. All units may be expanded to full capacity at any time by addition of plug-in printed circuit cards, without wiring changes or additions. All models of the Series 844 and 845 Multiplexers may be operated as analog demultiplexers. In the demultiplexing version, it is only necessary to disable an output shunt switch.

modeling code

MODEL NUMBER XXX-X-XX MULTIPLEXER

ADDRESS CODE	CHANNEL CAPACITY MAX/INCREMENTS	CODE
Binary Coded Decimal	100/10	844
Binary	160/16	845

CHANNEL SELECTION	CODE
Addressable	A
Sequential	B
Add/Seq	E
Direct (844 only)	C

CONTROL LOGIC LEVEL*		CODE
"1"	"0"	
+6 v	0 v	01
0 v	+6 v	02
−6 v	0 v	03
0 v	−6 v	04

*Logic for input and output control signals

specifications

SERIES 844 AND 845 (A, B AND E MODELS)

SWITCH TYPE:	High level, single-ended, SPST, transformer driven. The common ground line for all channels is isolated from chassis, power and logic ground by more than 2000 megohms.
SIGNAL INPUT:	Nominal full scale input is ± 10 volts. An overvoltage of up to ± 50 volts can be tolerated across any switch without damage.
SIGNAL OUTPUT:	The output signal is identical to input signal within applicable specifications.
SAMPLING RATE:	50,000 channels/second, maximum.
CHANNEL "ON" TIME:	10 μsec minimum, 100 μsec maximum.
DUTY CYCLE:	The maximum duty cycle for any switch is 50%.
SOURCE RESISTANCE:	The maximum recommended source resistance is 1000 ohms.
LEAKAGE CURRENT:	± 2 na per switch at 25°C.
SWITCH IMPEDANCE:	An "ON" switch has an impedance of 50 ± 20 ohms. An "OFF" switch has an impedance of 2000 megohms minimum shunted by 15 pf maximum.
LOAD IMPEDANCE:	The recommended load is 50,000 ohms shunted by 500 pf maximum.
LINEARITY:	The maximum departure from the best straight line of input vs output is less than ± 0.01% of full scale for signal currents of ± 0.25 ma or less.
OFFSET:	Less than ± 0.25 mv at 25°C ± 5°C. Less than ± 1.0 millivolt over the operating temperature range (— 10°C to + 55°C).
CROSSFEED:	For d-c signals the worst case crossfeed is $<\pm$ 0.001% of full scale. For a-c signals (f>4 cps), the worst case crossfeed, in percentage of full scale, is given by the approximate equations: Series 844 A, B and E Models Crossfeed, % FS = $7.6 \times 10^{-9}(8 + N) R_S f$ Series 845 A, B and E Models Crossfeed, % FS = $7.6 \times 10^{-9}(14 + N)R_S f$ f = signal frequency, cps R_S = source resistance, ohms N = number of switch **cards**
SETTLING TIME:	The output is within 0.01% of final value in $< 5 + 6 \times 10^{-6} R_S[250 + C_L + (N\text{-}1)15]$ μsec R_S = source resistance, ohms C_L = load shunt capacitance, picofarads N = number of switch **cards**
OPERATING TEMPERATURE:	— 10°C + 55°C, ambient
POWER:	105-125 vrms, 48-62 cps, single phase, 30 watts, max. 230 vrms available option.

SERIES 844 (C MODELS) Specifications identical to above except for:

SAMPLING RATE:	57,000 channels/second, maximum.
SWITCH IMPEDANCE:	An "ON" switch has an impedance of 25 ± 10 ohms. An "OFF" switch has an impedance of 2000 megohms minimum shunted by 15 pf maximum.
OFFSET:	Less than ± 0.13 millivolt at 25°C ± 5°C. Less than ± 0.5 millivolt over the operating temperature range (—10°C to + 55°C).
CROSSFEED:	For d-c or low-frequency signals, the worst case crossfeed as a percentage of full scale is given by the approximate equation: Crossfeed, % FS = $5 \times 10^{-8}(n\text{-}1)R_S$ For a-c (f>4 cps), the worst case crossfeed is given by the approximate equation: Crossfeed, % FS = $7.54 \times 10^{-9}(n\text{-}1)R_S f$ f = signal frequency, cps R_S = source resistance, ohms n = number of switch **channels**
SETTLING TIME:	The output is within 0.01% of final value in $< 5 + 6 \times 10^{-6} R_S[100 + C_L + (n\text{-}1)15]$ μsec R_S = source resistance, ohms C_L = load shunt capacitance, picofarads n = number of switch **channels**

controls and control signals

SERIES 844 AND 845 (A, B AND E MODELS)

ADDRESSABLE Indicator Lamp (E Models only) — Glows when unit is in addressable mode.

SEQUENTIAL Indicator Lamp (E Models only) — Glows when unit is in sequential mode.

ADD., SEQ., EXT., TEST Mode (E Models only) — Four-position rotary switch selects modes:

SAMPLE — Pushbutton switch provides a single clock pulse.

RESET — Pushbutton switch. Clears channel register to zero.

INT-EXT CLOCK—Two-position rotary switch. Selects self-contained clock or externally supplied clock for control.

Test Points — Test points located on front panel for channel (clock) and frame sync and multiplex output. D-C power voltage test points available on rear panel.

A-C Line — 3 prong a-c power connector.

Output — Multiplexed signal output connector.

(MODEL 845 E SHOWN)

Channel Number Display — A front panel in-line display of the selected channel number.
Model 844: Two digit decimal.
Model 845: Three digit octal.

Manual Channel Select — Front panel in-line switches to select any channel in TEST mode only.
Model 844: Two digit decimal.
Model 845: Three digit octal.

Frame Length (SEQUENTIAL Mode Only)— On sequential models, in-line switch setting determines frame length.

Power— An "off-on" switch located on the front panel with power fuse and pilot lamp.

Input Signals — Connectors on rear of switch cards protruding through rear panel.

Control Signals — Connectors on rear of logic cards protruding through rear panel.

control signal input requirements

Certain similarities in control signals exist between the various models. A general description of the operation and input signal requirements follows:

ADDRESSABLE UNITS (A Models) These units require an *Eight-line Single Rail Address* (BCD for Model 844, binary for Model 845) plus an *Address Set* signal. The set signal may be applied simultaneously with the address or at any time after the address is established. The channel sampling period is normally initiated 1.5 μsec after the set signal, but may be controlled by an external clock *(Sample Initiate)* signal.

SEQUENTIAL UNITS (B Models) The *External (or Internal) Clock* signal initiates the sampling period of the channel selected by the channel sequencing register. At the termination of the sampling period the register is internally advanced to the next (sequential) channel. The register may be cleared to zero at any time by applying a *Reset* signal to the reset input.

COMBINATION UNITS (E Models) These units require a *Mode Select* signal which directs the control logic to operate in the sequential or addressable mode; a true or "1" signal selects addressable and a false or "0" signal selects sequential. The mode may be selected automatically (when the front panel switch is in *External* position) or manually.

control signal output capabilities (E-model as example)

MODE CONFIRMATION A true or "1" level is supplied when unit is operating in addressable mode, a false or "0" level when in sequential mode.

SAMPLE INITIATE READY A true or "1" level is supplied when the unit is ready to accept a sample initiate command.

ADDRESS SET READY A true or "1" level is supplied when the unit is ready to accept an address set command.

CHANNEL NUMBER CONFIRMATION An eight-line single rail output (BCD for Model 844, binary for Model 845) indicating which channel is being sampled.

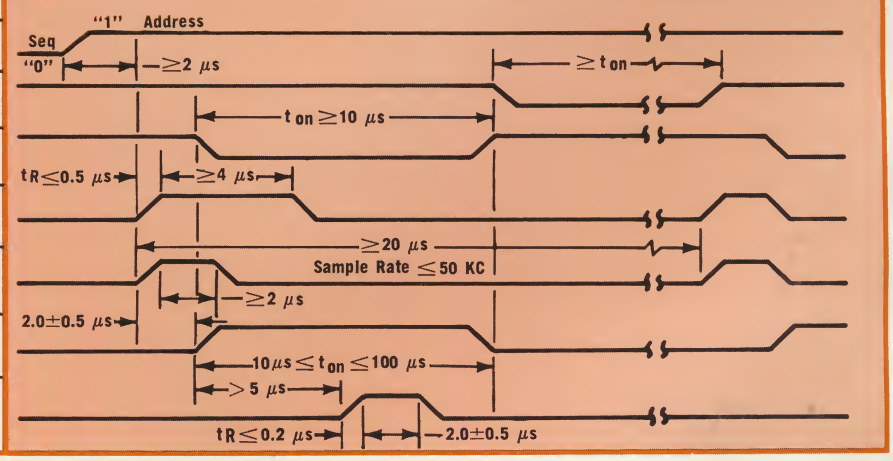
CONVERT ENABLE A true or "1" pulse normally supplied 5.5 ± 0.5 μsec after the clock signal. May be used to start an A-D Converter.

CLOCK SYNC A true or "1" pulse, occurring approximately 1.5 μsec after internal or external clock, indicates that register is set, sampling period may be initiated, and that address confirmation output is available.

FRAME SYNC A true or "1" pulse occurring synchronously with clock sync whenever the channel register contains zero.

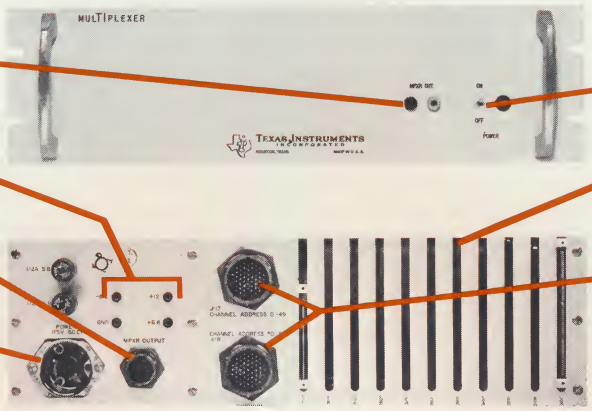
input/output control timing diagram (E-model shown)

Input	Output	Model A	Model B	Model E
MODE SELECT				√
	SAMPLE INITIATE READY	√	√	√
	ADDRESS SET READY	√		√
CHANNEL ADDRESS		√		√
SAMPLE INITIATE (or ADDRESS SET)		√	√	√
	CHANNEL "ON"	√	√	√
	CONVERT ENABLE	√	√	√



controls and control signals

SERIES 844 (C MODELS)



Test Output — Test points are located on the front panel for the multiplexed output signal.

Test Points — D-C power voltage test points are available on rear panel.

Output — Multiplexed signal output connector.

A-C Line — 3 prong a-c power connector.

Power — An "off-on" switch located on the front panel with pilot lamp.

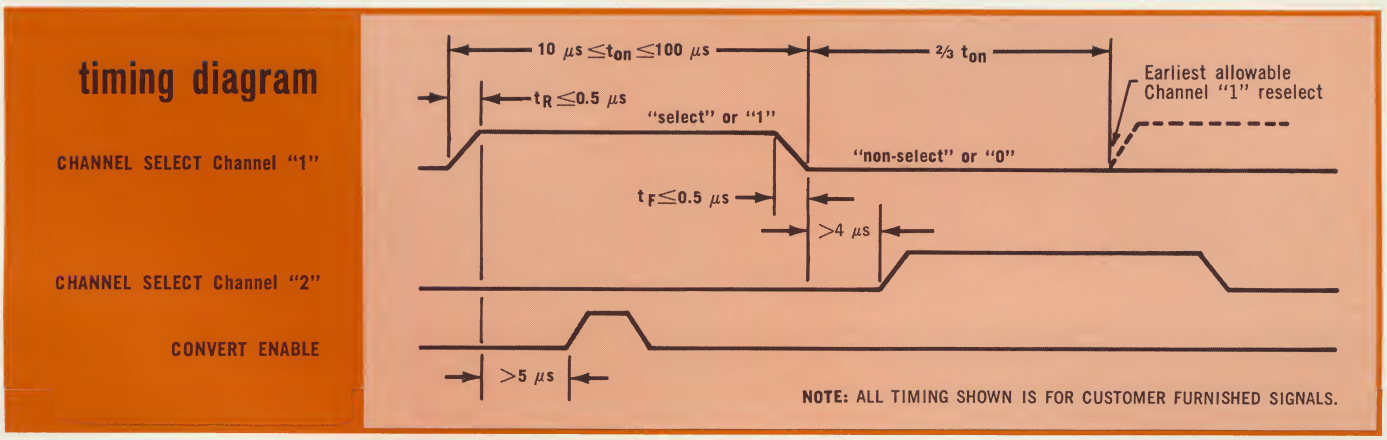
Input Signals — Connectors on rear of switch cards protruding through rear panel.

Channel Select Lines — Connectors for 100 individual channel select lines.

operation and control

For those applications where already decoded individual address lines are available, the 844C Direct Select Multiplexer affords a straightforward solution to channel selection. Each channel has its select line; no sequencing, addressing, or control logic is included. As shown above there are no channel select or frame length switches and no channel number displays on the front panel. The Model 844C includes switch cards, service extender module, and power supply in a slide-mounted case.

timing diagram

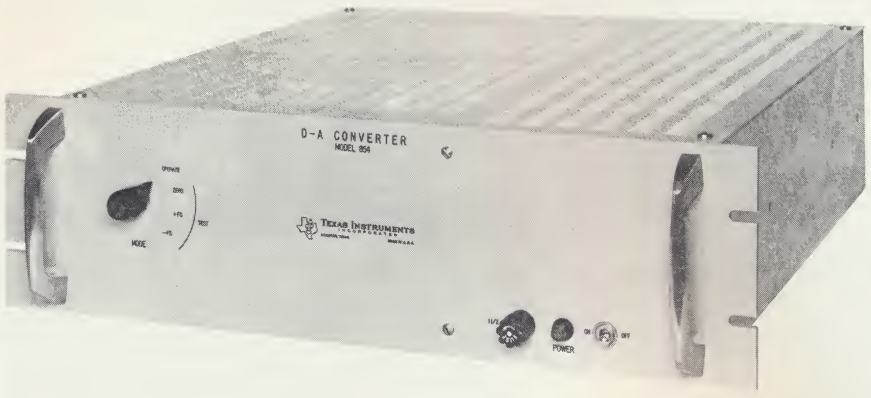


control signal specifications (all models)

Control Input Requirements		Control Output Capability	
Logic Levels:	See Model Chart	Logic Levels:	See Model Chart
Tolerance:	± 1 v	Tolerance:	± 1 v
Rise Time:	≤ 0.5 μsec	Rise Time:	≤ 0.5 μsec with 1000 pf load
Width:	≥ 2 μsec (≥ 4 μsec for **Channel Address**)	Fall Time:	≤ 0.5 μsec
Fall Time:	≤ 0.5 μsec	Max Current:	± 6 ma at either level
Max Current:	± 2 ma at either level		
Logic Load:	≥ 2700 ohms shunted by 250 pf		

SERIES 854

digital to analog converters



- High Speed—to 500,000 conversions/sec
- High Accuracy—to ± 0.01% full scale
- Digital Demultiplexing Capability
- Individual Input Holding Register

The Texas Instruments Series 854 Digital to Analog Converter is a versatile solid-state unit providing accurate high speed conversion of digital data from 8 to 14 bits in word length. The system is designed such that a number of independent D-A converters (6 to 12) can be mounted in a single chassis. Each channel has its own digital data register, switch and ladder, and optional output amplifier; each channel can operate at a conversion rate of 500 KC maximum without amplifier, 200 KC maximum with output amplifier. The chassis is wired for the maximum complement of channels and includes the digital and reference power supplies. A front panel switch provides zero, minus full scale, or plus full scale to all channels facilitating system calibration and checkout.

By means of a driver card and individual channel *Register Set* lines, digital demultiplexing of data can be accomplished. Because of the digital holding register, analog outputs can be held constant for as long a period as desired with no decay in accuracy.

The basic number system for instruments in this series is offset binary with two's complement and unipolar models available.

modeling code

MODEL 854 – XXX – XXX – X D-A CONVERTER

BASIC SERIES

NUMBER OF CHANNELS

BASIC SPEED AND ACCURACY WITHOUT AMPLIFIER			
INPUT INCLUDING SIGN	MAXIMUM CONVERSION RATE PER SECOND	ACCURACY	CODE
10 binary bits	500 KC	±0.1% FS	A
12 binary bits	500 KC	±0.025% FS	B
13 binary bits	500 KC	±0.025% FS	C
14 binary bits	500 KC	±0.01% FS	D
8 binary bits	500 KC	±0.2% FS	E

LOGIC LEVELS		CODE
"1"	"0"	
+6 v	0 v	01
0 v	+6 v	02
−6 v	0 v	03
0 v	−6 v	04
+10 v	0 v	11
0 v	+10 v	12
−10 v	0 v	13
0 v	−10 v	14

OUTPUT	CODE
High impedance—no amplifier, ±5 v, R_O = 1 K ohm	A
Low impedance—noninverting amp, ±10 v, ±20 ma, R_O = 0.1 ohm	B
Low impedance—inverting amp, ±10 v, ±20 ma, R_O = 0.1 ohm	C

INPUT TYPE	CODE
Single-rail Driver card required	1
Double-rail No driver required	2

NUMBER SYSTEM	CODE
Offset Straight Binary	A
Two's Complement	C
Unipolar	D

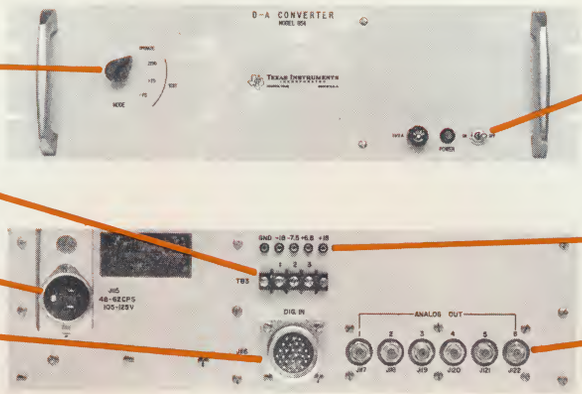
controls and control signals

MODE Switch—Four position rotary switch selects operating mode or any of three test modes

Terminal Block—Isolated analog and chassis grounds available on rear panel

A-C Line—3 prong a-c power connector

Input Signals—Digital Input and *Register Set* signal input connector



Power—An "OFF-ON" switch located on the front panel with power fuse and pilot lamp

Test Points—D-C power voltage test points available on rear panel

Output Signals—Analog signal outputs brought to separate connectors

specifications

DIGITAL DATA INPUT:

Single rail, parallel entry to register.

For multichannel DACs sharing a common source of digital data, digital demultiplexing of the data is possible. Parallel data is entered into a driver card which in turn drives all DAC channels (up to 12) in a chassis. The data is entered into the register of only one DAC channel, that one being denoted by a "1" signal on the appropriate channel *Register Set* line; all other DACs ignore the data.

For multichannel DACs having independent sources of digital data, the driver card may be removed. Double rail entry to each channel is thus required; the *Register Set* signal to each channel is still required.

LOGIC LEVELS:

Available logic levels of data (Digit Input) and *Register Set* are given in Modeling Code Chart.

CODE FORMAT:

Number of bits and binary code type are given in Modeling Code Chart.

INPUT IMPEDANCE:

Digit Input:

Single rail (with driver card): 6.2 K ohm shunted by 220 pf
Double rail (without driver card): 6.2 K ohm

Register Set Input: 6.2 K ohm shunted by 220 pf

CONTROL SIGNAL INPUT REQUIRED (from customer):

Operation to 200 KC:

Digit Input signals must occur 1.5 μsec or more before *Register Set* signal. Trailing edges of both signals may coincide.

Digit Input:
Rise Time: $\leqq$ 0.5 μsec
Width: $\geqq$ 2.0 μsec

Register Set:
Rise Time: $\leqq$ 0.5 μsec
Width: $\geqq$ 0.5 μsec

Operation to 500 KC:

Attainable with high impedance output only.
Digit Input signals must occur 1.0 μsec or more before *Register Set* signal. Trailing edges of both signals may coincide.

Digit Input:
Rise Time: $\leqq$ 0.1 μsec
Width: $\geqq$ 1.2 μsec

Register Set:
Rise Time: $\leqq$ 0.1 μsec
Width: $\geqq$ 0.2 μsec

ANALOG DATA OUTPUT:

High impedance output is available directly from ladder.
Voltage: $\pm$ 5.0 volts
Resistance: 1000 ohms $\pm$ 0.02%
Accuracy: As given in Modeling Code Chart
Settling Time: $\leqq$ 1 μsec to 0.05% of final value

Low impedance output is through inverting or noninverting amplifier.
Voltage: $\pm$ 10.0 volts
Current: $\pm$ 20.0 ma
Resistance: $\leqq$ 0.1 ohm
Accuracy: $\pm$ 0.05% of full scale
Offset: $\leqq$ 2.0 mv
Settling Time: $\leqq$ 5 μsec to within 0.05% final value

TEST CAPABILITY:

By means of front panel selector switch, positive and negative full scale and zero signals can be entered into all channels for alignment. Each amplifier has zero and gain adjustment for trimming.

PHYSICAL DETAILS:

Chassis assembly includes built-in power supply, plug-in reference supply and driver card. All solid-state, plug-in printed circuit cards. Maximum channel capacity per chassis:

No. of Bits	w/o Amplifier	w/Amplifier
8	12	8
10 & Up	6	6

OPERATING TEMPERATURE:

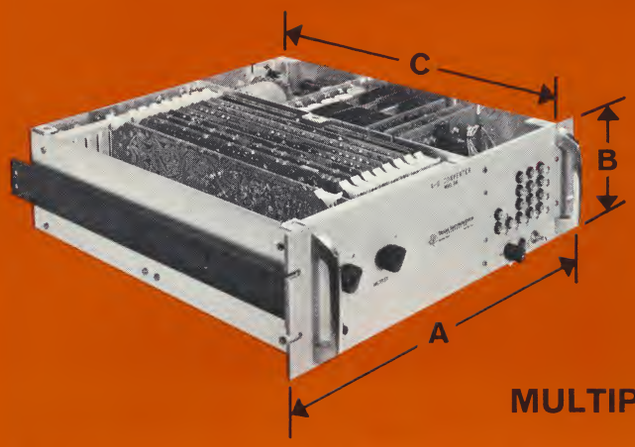
0°C to 55°C

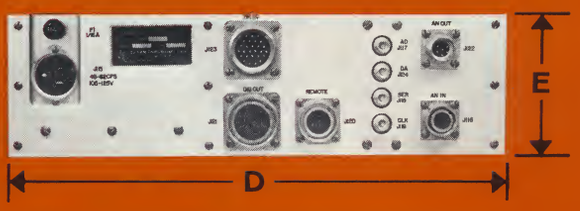
POWER:

105-125 vrms, 48-62 cps, single phase, 80 watts, max. 230 vrms available option.

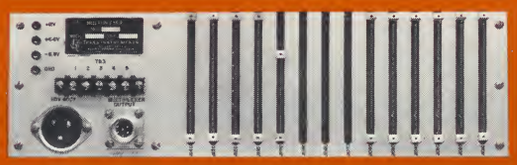
construction details

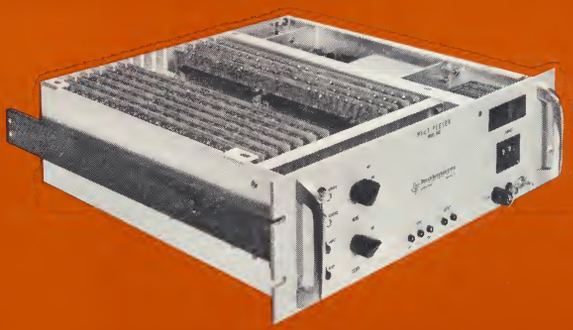
ANALOG TO DIGITAL CONVERTER



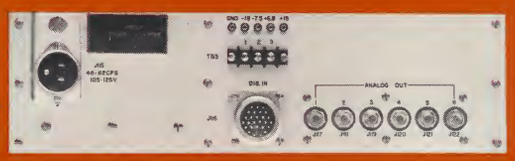


MULTIPLEXER





DIGITAL TO ANALOG CONVERTER



dimensions and weight

		AD Converter Series 846	Multiplexer Series 844/845	DA Converter Series 854
Dimensions	A	19 in.	19 in.	19 in.
	B	5¼ in.	5¼ in.	5¼ in.
	C	17⅝ in.	18 in.	17⅝ in.
	D	17 in.	17 in.	17 in.
	E	5⅜ in.	5⅜ in.	5⅜ in.
Weight		40 lb	30 lb	40 lb
Front Panel Finish		TI Beige #749. FED-STD 595 bake-on enamel, any color, available as extra cost option		
Mounting Provision		Standard rack mount with pull-out slides included		

INDUSTRIAL
PRODUCTS
GROUP

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